Engr433

Xilinx Tool Introduction

Schematic Based Design Entry

Revised 10/8/2019

- Logon to the Linux system. Open a terminal window and create a class directory, change to your new directory, and create another new directory entitled lab3. Cd into the lab3 directory. Useful commands: mkdir, cd
- 2. Start the Xilinx version 14.7 *integrated software environment* (ISE) software by entering **ise** at the command prompt and pressing enter (note the command is lower case). ISE may start up with a prior design loaded. If so, click **File** on the tool bar and select **close**. Click **OK** in the *Tip-Of-The-Day* window.



- 3. Four "buttons" are displayed in the upper left. Create a new project by clicking on the **New Project...** button:
 - a) A *New Project Wizard* pop-up window will open. The path to a prior project may be shown. Before entering the name of a new project, select the directory where the new project will be created. Click the little box with dots (...) to the right of the **Location** field and navigate to the desired directory where you wish to place your design.

Page 2

>	New Project Wizard	- + ×
Create New Project Specify project lo	t cation and type.	
Enter a name, loca	tions, and comment for the project	
N <u>a</u> me:	demo1circuit	
Location:	/home/aamola/ee433/fall15/demo1/demo1circuit	
Working Directory:	/home/aamola/ee433/fall15/demo1/demo1circuit	<u></u>
Description.		
Select the type of t	op-level source for the project	
Schematic	pe:	•
<u>M</u> ore Info	<u>N</u> ext >	Cancel

- b) Type in a project name (it will show up in the Location field also as you type). I suggest using demolcircuit as shown above.
- c) Select Schematic as the top-level source type for the project.
- d) Click Next.
- e) The *Project Settings* screen should appear. Set it up as follows:

Evaluation Dev Board:	None specified
Product Category:	General Purpose
Family:	Spartan6
Device:	XC6SLX16
Package:	FTG256
Speed:	-3
Top-level Source Type:	Schematic (this field may be grayed out. That's ok.)
Synthesis Tool:	XST (VHDL/Verilog)
Simulator :	ISim (VHDL/Verilog)
Preferred Language:	VHDL
Property specification:	Store all values

- f) Click Next.
- g) The *Project Summary* screen should appear. Look over the information. If something is not as you desire then use the **Back** button to go back and make a correction. Otherwise click **Finish**.
- h) In the upper left of the screen is a box with the word Hierarchy at the top. Just left of that



is a row of iconic buttons. The top icon is New Source. Click on it.

 The *New Source* wizard window should appear. Click on Schematic and then type in a file name. I suggest using a descriptive name but for the purposes of this tutorial, use *top_schematic*. Since designs can be created hierarchically, this naming convention will make clear that this is the highest level of your design and is a schematic type design block. Click Next. The *New Source Wizard Summary* will be displayed. Click Finish.

> New Source	Wizard - + ×
Select Source Type Select source type, file name and its loc	ation.
 IP (CORE Generator & Architecture Wizai Schematic User Document Verilog Module Verilog Test Fixture VHDL Module VHDL Module VHDL Library VHDL Package VHDL Test Bench Embedded Processor 	File name: top_schematic Location: pola/ee433/fall15/demo1/demo1circuit
	Add to project
More Info	Next > Cancel

j) You may be told that the directory xxx/nnnnn (xxx represents a path string) does not exist, would you like to create it? Answer **yes**.

Page 4

4. A blank schematic sheet should appear in the right 2/3 of the ISE window. On the left you should see a sub-window with several tabs near the bottom. Tabs include **Start, Design, Files, Library, Symbols, Options**.



a) Right click on the schematic in the right window and then click **Object Properties** at the bottom of the pop-up menu. A sheet size of 22x17 (C size) will be shown. Click on C=22x17 which should open a list of sheet sizes. For your first design click on A=11x8.5 and then click OK. The screen will likely show a grid of dots. Note that for larger designs you will want to use a B or C size sheet.

Page 5

Edit View Project Source Process Add Tools Wi	ndow La <u>y</u> ou	t <u>H</u> elp	-
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Select the entire branch	►	<u>^</u>	
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- 5. The next task is to create a simple circuit. The circuit will be an external signal coming in to an inverter and then going out again. Three circuit components (*ibuf, inv, obuf*) and two connectivity symbols for specifying connections to the outside world will be required.
 - a) Click on the **Symbols** tab at the bottom of the left subwindow. Two smaller windows should open with the top labeled *Categories* and the lower *Symbols*.
 - b) Click on category General and symbol Title. Move the cursor right and a title block will move over the schematic sheet. Move it towards the lower right corner of the sheet and left-click to place it. Hit the Escape key to un-connect the cursor from the symbol. Grab the top edge of the title block by positioning the cursor over it and holding down the left mouse button. Move the symbol tight into the lower right corner of the sheet and release.
 - c) Next, you are going to place components on the schematic. In the *Categories* window click on **IO** (scroll if needed). Find **ibuf** (input buffer) in the *Symbols* window below and left-click. Move your cursor to a location toward the left of the schematic sheet and centered vertically above the title block. Left-lick once.
 - d) Repeat for **obuf** and align it horizontally with **ibuf** but to the right with enough space in-between to place an inverter on the sheet.
 - e) In the *Categories* window select **Logic** and in the *Symbols* window find **inv** and place it between *ibuf* and *obuf*.





- f) Next, the inverter needs to be wired to the input and output buffers. Along the left edge of the schematic window is a *Tool bar*. Select the third icon down, the **Add Wire** tool. On the schematic, single left-click to start a wire and double left-click to end it.
- g) Next, I/O markers must be added to the *ibuf* input and *obuf* output. On the tool bar at the left of the schematic, select Add I/O Marker (7th icon down). In the Add I/O Marker Options panel on the left, click the Add an Input Marker option. Then, left-click on the end of the wire going into the *ibuf*. Next, select the Add an Output Marker option from the panel at the left and left-click on the end of the wire coming out of the *obuf*.
- h) Default net names start with XLXN which is cryptic. Change the value of the Name attribute to reflect the signal usage by double left-clicking on an I/O marker. When the I/O marker's object properties dialog box appears, select the Nets category and enter a meaningful value in the Name field of the I/O marker. I suggest *in1* and *out1* for our example circuit. Then click OK.



i) Next, we need to map our input and output signals to actual physical pins on the FPGA where we will implement our design. Double-click on the *in1* I/O marker and an Object Properties window will open. On the left under Category, click on Nets. Towards the right of the window click on the New button. A New Attribute window will open with the default attribute name of LOC. For Attribute value, type in a P9 (switch 0 on the FPGA board). Click OK.

ø	New A	ttribute	- + ×
Attrib	ute name		
LOC			_
Attrib	ute value		
P2			
Attrib	ute value t	ype	
String	1		-
☐ Rer	nember thi	is attribute na	ame
	ОК	Cancel	Help

- j) Repeat for the other I/O marker. Assign *out1* the Attribute value of L14 (LED 0 on the FPGA board).
- 6. When all parts are added and wired up you can do what is called *Design Rule Check* (DRC) of the schematic. This check does not tell you that the circuit will work, only that signals are connected to component inputs, etc. Messages from the DRC check are displayed in the transcript window at the bottom of the screen. DRC knows nothing about what your circuit is supposed to do.
 - a) From the tool bar at the left of the schematic click on the check mark symbol, 6th up from the bottom. Fix any errors or warnings that it flags.
- 7. Next you will synthesize the FPGA configuration information from the schematic you have entered.
 - a) First, set up a display of useful information. Under the schematic, click the tab labeled **Design Summary**. Then from the lower left tabs click on **Design**.
 - b) Next, on the horizontal tool bar at the top is a green arrow symbol, the Implement Top Module button. Left-click the green arrow. It may ask if you wish to save changes. If you don't save, it will use the design as it was prior to your last edit. This step will take some time. There can be several seconds delay from when you click and when new info appears on the screen while the program code is downloaded from the server and run. There are several different programs that run. Information will scroll by in the transcript window if it is open and the Design Summary window will update. Watch the sequence of results as synthesis, place, and route occur.
 - c) Finally, in the lower left window double-click **Generate Programming File** to generate the bit map file that will be downloaded to configure the FPGA.

ISE Project Navigator (P.20131013) - /home/aamola/ee433/fall15/demo1/demo1circuit.vise - [Design Summary (Programming File Generated)] - + × The File Set Now Project Course Researce Table Window Lowert Liele File Set Now								
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C3s250e-5vq100	Pinout Report Static Timing	Target Device: xc3	3s250e-5vq100	• Errol	's:	No Errors		_
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		Translation Report	Current	Tue Oct 6 13:09:12 2	015 0	0	0	
		Map Report	Current	Tue Oct 6 13:09:21 2	015 0	1 Warning (1 net	<u>N)</u> 2 Infos (2 ne	<u>w)</u>
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Process "Generate Programming File" completed successf	ully							
4								<u> </u>
Console C Errors 🔬 Warnings 🗟 Find in Files Results								

8. Downloading your design to the FPGA

At this point, make sure that the programming cable is connected between computer and FPGA board and then apply power to the FPGA board. Double-click **Configure Target Device** to start the iMPACT program. A Project Navigator window may open warning that no iMPACT project file exists. Click **OK**. The initial screen may look like this:

Page	9
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8	ISE IMPAC	T (P.20131013)	- + ×
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Double-click on **Boundary Scan**. The larger area to the right should turn white with a message "Right click to add device". Right-click and in the pop-up box that appears select **Cable Setup...** The cable setup box looks like this:

If not already selected, select Digilent USB JTAG Cable and then Click OK.

Cable Communication Setup	- + ×					
Communication Mode						
C Parallel Cable III C Platform Cable USB	C Parallel Cable III C Platform Cable USB/II					
C Parallel Cable IV C Digilent USB JTAG C	able					
C HW Server						
Advanced USB Cable	Setup					
Port: TCK Speed/Baud	Rate:					
JtagHs2/210249A0D649 🔽 Default Speed	•					
Cable Location						
6 local						
Host Name:						
C Remote						
Cable Plug-in						
Copen Cable Plug-in. Select or enter a Plug-in fron						
atformusb PORT=USB21 FREQUENCY=6000000						
OK Cancel H	elp					

Page 10

Again, right-click on the large white window to the right and select **Initialize Chain**. The right window should look something like this:



A pop box will ask this:

🛞 🛛 Auto Assign Configuration Files Query Dialog 👘 – + 🗙
Do you want to continue and assign configuration files(s)?
☐ □ Don't show this message again, save the setting in preference.
Yes <u>N</u> o

Click Yes. Configuration filenames have a .bit extension. Navigate if needed to the correct directory where your *top_schematic.bit* file is located and double-click it.

	Page 11					
	Assign New Configuration File	•				- + ×
Look in:	<pre>/home/aamola/ee433/fall16/fpga2_test1 ngo xmsgs iseconfig xlnx_auto_0_xdb xst fpga2_test1.bit toplevel.bit</pre>	•	0	•	0	
File <u>n</u> ame: Files of type:	fpga2_test1.bit All Design Files (*.bit *.rbt *.nky *.isc *.bsd)				•	Open Cancel Bypass Cancel All

Because there is a second part on the FPGA board a window like this may appear:

₿	Attach SPI or BPI PROM - + ×
?	This device supports attached Flash PROMs. Do you want to attach an SPI or BPI PROM to this device?
	Yes <u>N</u> o

Click No. (you don't want to down load to the PROM memory chip).

Even though you said **No** to attaching the SPI memory part, a window like this may open as if to allow selection of a data file to be downloaded to memory. **Click Bypass**:

Page 12

	Assign New Configuration File				-	+ :	×
Look in:	<pre>/home/aamola/ee433/fall16/fpga2_test1_250 ngo xmsgs iseconfig xlnx_auto_0_xdb xst</pre>	G	0	•		:: :	
File <u>n</u> ame:					O Ca By	pen ncel pass	
Files of type:	All Design Files (*.mcs *.isc *.bsd)			•	Cano	cel All	

The next window is titled **Device Programming Properties**. It may state that there are no applicable properties for this device. Just click **OK**.

Device Programming Prop	perties - Device 1 Programming Properties – +	×
<u>C</u> ategory		
🖻 Boundary-Scan		_
Device 1 (FPGA xc3s250e)	Property Name Value	
Device 2 (PROM xcf02s)	Verify 🗖	
	FPGA Device Specific Programming Properties	
	Pulse PROG	
,		
	OK Cancel Apply Help	

You are now ready to download the *top_schematic.bit* file to the FPGA. In the lower left window double-click **Program**. Or right-click on the FPGA in the right window. The FPGA will now contain your design. Before exiting *iMPACT*, I recommend that you do a cable disconnect under *Output* on the tool bar. (Disconnect All Cables).